UNIT 4
BIASING AND STABILIZATION

TRANSISTOR BIASING:

To operate the transistor in the desired region, we have to apply external dc voltages of correct polarity and magnitude to the two junctions of the transistor. This is known as biasing of the transistor.

Since DC voltages are used to bias the transistor, it is called as DC biasing.

DC OPERATING POINT (OR) QUIESCENT POINT:

Application of DC voltages (bias) establishes a fixed level of current and voltage. For transistor amplifiers the resulting DC current and voltage establish an operating point on the characteristics that define the region that will be employed for amplification of the applied signal. Since the operating point is a fixed point on the characteristics, it is called as Quiescent point (Q-Point).

Note: Quiescent → Still inactive and quiet.

NEED FOR BIASING:

→ To operate the transistor in the desired region.
→ The DC sources supplies the power to the transistor circuit, to get the output signal power greater than the input signal power.

LOAD LINE:

→ It is a straight line drawn on the characteristic curve with two end points A and B.
→ It is used to fixed the operating point of a transistor.

TYPES OF LOAD LINE:

→ DC load line
→ AC load line
DC LOAD LINE:
Consider the common emitter amplifier circuit shown.

Step (1): Remove the ac signal, so that the circuit becomes.

Step (2): Draw the graph of $I_C$ vs $V_{CE}$ (i.e., output characteristic curve).

Step (3): Find the two end points of the straight line.
For that, Apply KVL to the collector circuit.

\[ V_{CC} = I_C R_C + V_{CE} \rightarrow 1 \]

W.k.t the equation for straight line is
\[ y = mx + c \]
Here
\[ y = I_C \]
\[ x = V_{CE} \]
From equation (1),
\[ I_C R_C = V_{CC} - V_{CE} \]
\[ I_C = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C} \rightarrow 2 \]

To find A:
A is a point on X-axis
Put Y = 0, ie \( I_C = 0 \) in equation 2
\[ 0 = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C} \]
\[ V_{CE} = V_{CC} I_{IC=0mA} \]

To find B:
B is a point of Y – axis
Put X = 0, ie \( V_{CE} = 0 \) in equation 2
\[ I_C = \frac{V_{CC}}{R_C} I_{V_{CE}=0} \]
Finally plot the points A & B on the curve.

Step(4):
Select the \( I_B \) curve so as to find the Q – point.

To find \( I_B \):
Apply KVL to base circuit.
\[ V_{CC} = I_B R_B + V_{BE} \]
\[ I_B = \frac{V_{CC} - V_{BE}}{R_B} \]

For silicon transistor \( V_{BE} = 0.7V \)
If \( V_{CC}, R_B \) is known, the value of \( I_B \) can be found.
**Example:**

\[ V_{CC} = 20V, \, R_B = 5K, \, I_B = 3mA \]

**Conclusion:**

Thus the intersection of DC load line and \( I_B \) curve is called as Q – Point.

**Problem:**

Find the Q-point for the given circuit:

\[ V_{CC} = 20V, \, B = 49, \, R_E = 100\, \Omega, \]

\[ R_B = 5K, \, V_{CC} \]
Solution:

Step (i):

Remove the AC source and redraw the circuit.

Step (2):

To find A & B points:

To find A & B:

Apply KVL to collector circuit.

\[ V_{cc} = I_c R_C + V_{CE} + I_E R_E \]

\[ V_{cc} = I_c (R_C + R_E) + V_{CE} \]

From CKT,

\[ I_E = I_B + I_C \]

\[ I_E = I_C \]

\[ I_E \ll I_C \]

\[ I_C = \frac{V_{cc}}{R_C + R_E} - \frac{V_{CE}}{R_C + R_E} \]

Since A is a point of X-axis,

\[ I_C = 0 \]

\[ V_{CE} = V_{cc} | I_C = 0 \] (Point A)

Since B is a point of Y-axis,

\[ V_{CE} = 0 \]
\[ I_C = \frac{V_{CC}}{R_C + R_E} | V_{CE} = 0 \text{ (Point B)} \]

Step (3):

To find \( I_B \) curve.

Apply KVL to base circuit.

\[ V_{CC} = I_B R_B + V_{BE} + I_E R_E \]

\[ V_{CC} = I_B (R_B + (1 + \beta)R_E) + V_{BE} \]

\[ I_B = \frac{V_{CC} - V_{BE}}{R_B + R_E(1 + \beta)} \]

\[ I_B = \frac{20 - V_{BE}}{5 \times 10^2 + 100(1 + 49)} \]

\[ I_B = \frac{20}{5K + 5000} \]

\[ I_B = 2mA \]

Step (4):

**SELECTION OF OPERATING POINT FOR A.C INPUT SIGNAL:**

The operating point can be selected at three different positions on the DC load line:

→ Near saturation region
→ Near cut-off region
→ At the centre i.e. Active region
Case (1):

**NEAR SATURATION REGION:**

If the biasing circuit is designed to fix the Q – point (P) very near to saturation region, the collector current is clipped at the positive half cycle. Thus because of the distortions present at the collector current, point P is not the suitable operating point.

Case (ii):

**NEAR CUT-OFF REGION:**

If the biasing circuit is designed to fix the Q – point (R) near cut-off region, the collector current is clipped at the negative half cycle. Thus Q-point R is also not a suitable operating point.
Case(iii):

**AT ACTIVE REGION:**

If the Q-point is fixed at the centre of the active region, the output signal is sinusoidal waveform without any distortion. Thus the point Q is the best operating point.

![Graph of sinusoidal waveform](image)

**Bias stabilization:**

While designing the biasing circuit, case should be taken so that the operating point will not shift into an undesirable region (ie into cut-off or saturation region)

Factors to be considered while designing the basing circuit:

- Temperature dependent factors ($I_{CO}, V_{BE}$)
- $\beta | hfe$ – Transistor current gain

**$I_{CO}$:**

The flow of current in the circuit produces heat at the junctions. This heat increases the temperature at the junctions.

Since the minority carriers are temperature dependent ($I_{CO}$ gets doubled for energy $10^\circ$C raise in temperature), they increase with the temperature. This in turn increase the $I_C$ and hence Q-point gets shifted

**$V_{BE}$:**

- $V_{BE}$ changes with temperature at the rate of $2.5\text{mv}^\circ\text{c}$
- $I_B$ depends on $V_{BE}$

Since $\frac{I_C}{I_R} = \beta$

$I_C = \beta I_B$, increase in $I_B$

Increase $I_C$ This in turn changes the operation point.
Transistor current gain $\beta$:

The transistor parameters among different units of same type, same number changes. I.e. If we take two transistor units of same type (i.e. Same number, construction, parameter specified etc.) and we them in the circuit, there is change in the $\beta$ value in actual practice. The biasing circuit is designed according to the required $\beta$ value. Since $\beta$ changes, the operating point also shifts.

REQUIREMENTS OF A BIASING CIRCUIT:

→ The emitter-base junction must be forward biased and collector-base junction must be reversed biased. I.e. The transistors should be operated in the active region.
→ The circuit design should provide a degree of temperature stability.
→ The operating point should be made independent of transistor parameters (like $\beta$)
→ Techniques used to maintain the Q – point stable:

STABILIZATION TECHNIQUE:

This refers to the use of resistive biasing circuits which allow $I_E$ to vary so as to keep $I_C$ relatively constant with variations in $I_{CO}$, $\beta$ and $V_{BE}$

COMPENSATION TECHNIQUE:

This refers to the use of temperature sensitive devices such as diodes, transistors, thermistors, etc, which provide compensating voltages and current to maintain the operating point stable.

STABILITY FACTORS:

→ The stability factor is a measure of stability provided by the biasing circuit.
→ Stability factor indicates the degree of change in operating point due to variation in temperature.
→ Since there are 3 temperature dependent variables, there are 3 stability factors.

$$S = \frac{\Delta I_C}{\Delta I_{CO}} | V_{BE,\beta \text{ constant}} \quad \text{(or)} \quad S = \frac{\Delta I_C}{\Delta I_{CO}} | V_{BE,\beta \text{ constant}}$$
\[
S' = \frac{\partial I_C}{\partial V_{BE}} \mid_{I_{CO}, \beta \text{ constant}} \quad \text{(or)} \quad S' = \frac{\Delta I_C}{\Delta V_{BE}} \mid_{I_{CO}, \beta \text{ constant}}
\]
\[
S'' = \frac{\partial I_C}{\partial \beta} \mid_{V_{BE}, I_{CO} \text{ constant}} \quad \text{(or)} \quad S'' = \frac{\Delta I_C}{\Delta \beta} \mid_{V_{BE}, I_{CO} \text{ constant}}
\]

**Note:**
- Ideally, stability factor should be perfectly zero to keep the operating point stable.
- Practically stability factor should have the value as minimum as possible.

**EXPRESSION FOR STABILITY FACTOR S:**

For a common emitter configuration collector current is given by

\[
I_C = I_{C(majority)} + I_{CEO(majority)}
\]

WK

\[
I_{CEO} = \frac{I_{CBO}}{1 - \alpha}
\]

\[
I_{CEO} = (1 + \beta) \, I_{CBO}
\]

\[
I_C = \beta I_B + (1 + \beta) \, I_{CBO}
\]

When

- \(I_{CBO}\) changes by \(\Delta I_{CBO}\)
- \(I_B\) changes by \(\Delta I_B\)
- \(I_C\) changes by \(\Delta I_C\)

\[
\partial I_C = \beta \partial I_B + (1 + \beta) \partial I_{CBO}
\]

\[
\frac{1}{S} = \frac{\Delta I_B}{\Delta I_C} \quad \text{or} \quad S = \frac{\Delta I_C}{\Delta I_B}
\]

If \(S = \frac{\partial I_C}{\partial I_{CBO}}\)

\[
\frac{1}{S} = \frac{(1 - \beta) \partial I_B}{(1 + \beta) \partial I_C}
\]

\[
S = \frac{(1 + \beta) \partial I_B}{(1 - \beta) \partial I_C}
\]
TYPES OF BIASING CIRCUIT:

→ Fixed bias circuit
→ Collector to base bias circuit
→ Voltage divider or self bias circuit.

FIXED BIAS CIRCUIT:

To find $I_B$:

Apply KVL to the base circuit,

$V_{CC} = I_B R_B + V_{BE}$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \quad 1$$

$V_{BE} \ll V_{CC}$

$V_{BE} = 0.7 \text{ for si}$

$V_{CC} \rightarrow \text{fixed, } R_B \rightarrow \text{fixed and hence } I_B \text{ is fixed and the circuit is called as fixed bias circuit.}$

To find $V_{CE}$:

Apply KVL to the Collector circuit,

$V_{CC} = I_C R_C + V_{CE}$

$$V_{CE} = V_{CC} + I_C R_C \quad 2$$

To find $I_C$: 

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To find $I_B$:

Apply KVL to the base circuit,

$V_{CC} = I_B R_B + V_{BE}$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \quad 1$$

$V_{BE} \ll V_{CC}$

$V_{BE} = 0.7 \text{ for si}$

$V_{CC} \rightarrow \text{fixed, } R_B \rightarrow \text{fixed and hence } I_B \text{ is fixed and the circuit is called as fixed bias circuit.}$

To find $V_{CE}$:

Apply KVL to the Collector circuit,

$V_{CC} = I_C R_C + V_{CE}$

$$V_{CE} = V_{CC} + I_C R_C \quad 2$$

To find $I_C$: 

---
From equation (2),

\[ I_C = \frac{v_{CC} - v_{CE}}{R_C} \]  

\[ \rightarrow 3 \]

To find \( S \):

\[ WKT \]

\[ S = \frac{(1 + \beta)}{(1 - \beta)} \frac{\partial I_B}{\partial I_C} \]

\[ \frac{\partial I_B}{\partial I_C} = 0 \]

\[ S = \frac{(1 + \beta)}{(1 - \beta)} 0 \]

\[ \rightarrow 4 \]

To find \( S' \):

\[ S' = \frac{\partial I_C}{\partial V_{BE}} \]

\[ WKT, \]

\[ I_C = I_{C(majority)} + I_{CEO(majority)} \]

\[ I_C = \beta I_B + I_{CEO} \]

\[ I_C = \beta I_B + (1 + \beta) I_{CEO} \]

Sub \( I_B \) in above equation,

\[ I_C = \beta \left( \frac{v_{CC} - V_{BE}}{R_B} \right) + (1 + \beta) I_{CEO} \]

\[ \rightarrow 5 \]

Diff. \( I_C \) WRT to \( V_{BE} \)

\[ \frac{\partial I_C}{\partial V_{BE}} = \beta \frac{R_B}{v_{CC}} \]

\[ S' = \frac{-\beta}{R_B} \]
To find $S''$:

$$S'' = \frac{\partial I_C}{\partial \beta}$$

$$I_C = \beta I_B + (1 + \beta) I_{CBO}$$

$$I_C = \beta I_B + I_{CBO} + \beta I_{CBO}$$

Diff $I_C$ WRT to $\beta$

$$\frac{\partial I_C}{\partial \beta} = I_B + I_{CBO}$$

$$S'' = I_B + I_{CBO}$$

$$\boxed{S'' \approx I_B}$$

$$S'' = I_B = \frac{I_C}{\beta} \longrightarrow 6$$

To find relation between $s$ and $S'$

$$S = (1 + \beta)$$

$$S' = \frac{-\beta}{R_B}$$

To obtain $S'$ in terms of $S$

Multiply and divided by $(1 + \beta), S'$

$$S' = \frac{-\beta S}{R_B (1 + \beta)} \longrightarrow 7$$

To find relation between $S$ and $S''$

We have

$$S'' = \frac{I_C}{\beta}$$

$$S' = \frac{-\beta}{R_B}$$

Multiply and divided by $(1 + \beta), S''$

$$S'' = \frac{I_C}{\beta} \times \frac{(1 + \beta)}{(1 + \beta)}$$

$$S'' = \frac{I_C S}{\beta (1 + \beta)} \longrightarrow 8$$
ADVANTAGES OF FIXED BIAS CIRCUIT:

→ Circuit is simple
→ The operating point can be fixed anywhere in the active region by varying the value of $R_B$. Thus if provides maximum flexibility.

DISADVANTAGES:

→ Thermal stability is not provide by the circuit and so the Q-point varies

\[ I_C = \beta I_B + I_{CEO} \]

Since $I_C$ Q-point varies

→ Circuit depends on $\beta$

**Problem**

Design a fixed bias circuit using a silicon transistor having $\beta$ value of 100, $V_{CC} = 10V$ and DC bias condition are to be $V_{CE} = 5V$ and $I_C = 5mA$

**Solution:**

Given:
\[ \beta = 100 \]
\[ V_{CC} = 10V \]
\[ V_{CE} = 5V \]
\[ I_C = 5mA \]

To find:
\[ R_B = ? \]
\[ R_C = ? \]
\[ I_B = ? \]
To find $R_C$:

Applying KVL to collector circuit,

$$V_{CC} = I_C R_C + V_{CE}$$

$$10 = 5 \times 10^{-3} R_C + 5$$

$$\frac{5}{5 \times 10^{-3}} = R_C$$

$R_C = 1 \text{ K}\Omega$

To find $I_B$:

WKT $\frac{I_C}{I_B} = \beta$

$$I_B = \frac{I_C}{\beta}$$

$$= \frac{5m}{100}$$

$I_B = 50\mu A$

To find $R_B$:

Applying KVL to input circuit,

$$V_{CC} = I_B R_B + V_{BE}$$

$$10 - 0.7 = \frac{50\mu}{R_B}$$

$R_B = 1861 \text{ K}\Omega$

Design:
COLLECTOR TO BASE BIAS CIRCUIT:

Since the $R_B$ resistor is connected between the collector and base, it is called as collector to base bias circuit.

To find $I_B$:

Applying KVL to input circuit,

$$V_{CC} = (I_C + I_B)R_C + I_BR_B + V_{BE}$$

$$V_{CC} = I_CR_C + I_B(R_C + R_B) + V_{BE}$$

$$I_B = \frac{V_{CC} - I_CR_C - V_{CE}}{R_C + R_B} \quad \rightarrow 1$$

To find $V_{CE}$:

Applying KVL to output circuit,

$$V_{CC} = (I_C + I_B)R_C + V_{CE}$$

$$V_{CC} = V_{CC} - I_CR_C - I_BR_C \quad \rightarrow 2$$

To find $I_C$:

Applying KVL to collector circuit,

$$V_{CC} = (I_C + I_B)R_C + V_{CE}$$

$$V_{CC} = I_CR_C + I_BR_C + V_{CE}$$

$$I_B = \frac{V_{CC} - V_{CE} - I_BR_C}{R_C} \quad \rightarrow 3$$

WKT the basic equation for $I_C$ is
\[ I_C = \beta I_B + I_{CB0} \]
\[ I_C = \beta I_B + (1 + \beta) I_{CB0} \]

**\[ I_C \approx \beta I_B \]**

To find \( S \):

\[ S = \frac{(1 + \beta)}{(1 - \beta)} \frac{\partial I_B}{\partial I_C} \]

\( \frac{\partial I_B}{\partial I_C} \) is obtained by diff. \( I_B \) WRT \( I_S \)

\[ I_B = \frac{V_{CC} - I_C R_C - V_{BE}}{R_C + R_B} \]

\[ \frac{\partial I_B}{\partial I_C} = \frac{-R_C}{R_C + R_B} \rightarrow 4 \]

\[ S = \frac{(1 + \beta)}{(1 - \beta)} \frac{-R_C}{R_C + R_B} \]

\[ S = \frac{(1 + \beta) R_C}{(1 + \beta)(R_C + R_B)} \rightarrow 5 \]

\[ S = \frac{(1 + \beta)(R_C + R_B)}{R_C + R_B + \beta R_C} \]

\[ S = \frac{(1 + \beta)(R_C + R_B)}{R_B + (\beta + 1)R_C} \]

**To find \( S' \):**

\[ S' = \frac{\partial I_C}{\partial V_{BE}} \]

\[ I_B = \frac{V_{CC} - V_{BE} - I_B R_C}{R_C} \]

As there is no \( V_{BE} \) term in the above equation

WKT,

\[ I_C = \beta I_B \]

Sub \( I_B \) in above equation,
\[ I_c = \beta \left( \frac{V_{CC} - I_c R_c - V_{BE}}{R_c + R_B} \right) \]

\[ I_c = \frac{\beta (V_{CC} - V_{BE})}{R_c + R_B} - \frac{\beta I_c R_c}{R_c + R_B} \]

\[ I_c + \frac{\beta I_c R_c}{R_c + R_B} = \frac{\beta (V_{CC} - V_{BE})}{R_c + R_B} \]

\[ I_c R_B + I_c R_c + \beta I_c R_c = \beta (V_{CC} - V_{BE}) \]

\[ I_c = \frac{\beta (V_{CC} - V_{BE})}{R_c + R_B + \beta R_c} \quad \rightarrow \quad 5.1 \]

\[ I_c = \frac{\beta (V_{CC} - V_{BE})}{R_B + (1 + \beta) R_c} \quad \rightarrow \quad 6 \]

\[ \frac{\partial I_c}{\partial V_{BE}} = -\frac{\beta}{R_B} \]

\[ S' = \frac{-\beta}{R_B + (1 + \beta) R_c} \quad \rightarrow \quad 7 \]

**To find \( S'' \):**

\[ S'' = \frac{\partial I_c}{\partial \beta} \]

From equation (6),

\[ I_c = \frac{\beta (V_{CC} - V_{BE})}{R_c + R_B + \beta R_c} \]

\[ S'' = \frac{\partial I_c}{\partial \beta} \]

\[ = \frac{(R_c + R_B + \beta R_c)(V_{CC} - V_{BE}) - \beta (V_{CC} - V_{BE})(R_c)}{(R_c + R_B + \beta R_c)^2} \]

\[ S'' = \frac{(V_{CC} - V_{BE})(R_c + R_B)}{(R_B + (1 + \beta) R_c)^2} \quad \rightarrow \quad 8 \]

**To find relation between \( s \) and \( S' \):**

\[ S' = \frac{-\beta}{R_B + (1 + \beta) R_c} \]

Multiply and divided by \((1 + \beta) \), \(R_c + R_B\)
\[
S' = \frac{-\beta}{R_B + (1 + \beta)R_C} \times \frac{(1 + \beta)R_C + R_B}{(1 + \beta)R_C + R_B} \quad \Rightarrow \quad 8.1
\]

From equation (5),
\[
S = \frac{(1 + \beta)}{(1 - \beta)} \times \frac{-R_C}{R_C + R_B}
\]
\[
= \frac{(1 + \beta)R_C}{(1 + \beta)(R_C + R_B)}
\]
\[
S = \frac{(1 + \beta)(R_C + R_B)}{R_C + R_B + \beta R_C}
\]
\[
S = \frac{(1 + \beta)(R_C + R_B)}{R_B + (\beta + 1)R_C} \quad \Rightarrow \quad 9
\]

By combining equation (9) & (8.1),
\[
S' = \frac{-\beta S}{(1 + \beta)R_C + R_B} \quad \Rightarrow \quad 10
\]

To find relation between \( S \) and \( S'' \)

We have
\[
S'' = \frac{(V_{CC} - V_{BE})(R_C + R_B)}{(R_B + (1 + \beta)R_C)^2}
\]

Multiply and divided by \((1 + \beta)\) we have
\[
S'' = \frac{(V_{CC} - V_{BE})(R_C + R_B)}{(R_B + (1 + \beta)R_C)^2} \times \frac{(1 + \beta)}{(1 + \beta)}
\]
\[
S'' = \frac{(V_{CC} - V_{BE})S}{(1 + \beta)(R_B + (1 + \beta)R_C)}
\]
\[
S'' = \frac{I_C S}{\beta (1 + \beta)} \quad \Rightarrow \quad 11
\]

**ADVANTAGES:**

→ Circuit is flexible to fix the operating point at the centre of an active region.
→ Circuit is simple

→ \( S = 1 + \beta \) → Fixed bias
\[ S = \frac{(1+\beta)R_C}{(1+\beta)R_C + R_B} \rightarrow \text{For collector to base bias} \]

Thus \( S \) is small for collector to base bias circuit, hence this provides better stability than fixed bias circuit.

Q- Point is stable:

\[ I_C = \beta I_B + I_{CEO} \]

If \( \beta, I_{CEO} \) increases

\( I_C \) increases

Drop across \( R_C \) increases

\[ V_{CE} \text{ decrease } V_{CC} - I_C R_C + I_B R_C \]

\( I_R \) decrease \[ I_B = \frac{V_{CC} - V_{CE} - I_C R_C}{R_R} \]

\( I_C \) decrease \[ I_C = \beta I_B \]

Thus the original increase is compensated and Q – Point remains stable.
VOLTAGE-DIVIDER BIAS CIRCUIT: [OR] SELF–BIAS (OR) EMITTER BIAS CIRCUIT.

To find $I_E$:
Consider the closed loop shown in the circuit.

\[ V_B = V_{BE} + V_E \]
\[ V_B = V_{BE} + I_E R_E \]
\[ I_E = \frac{V_B - V_{BE}}{R_E} \rightarrow 1 \]

To find $V_{CE}$:
Applying KVL to the collector circuit.
\[ V_{CC} = I_C R_C + V_{CE} + I_E R_E \]
$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$ → 2

To find $V_{BE}$:

Redrawing the original circuit as follow,

To find thevenin’s equivalent circuit:-

To find $R_{th}(R_B)$:

$$R_{th} = \frac{R_1 R_2}{R_1 + R_2}$$ → 3
To find $V_T(V_{th})$:

$$V_T = \frac{V_{CC}R_2}{R_1+R_2} \rightarrow 4$$

By voltage divided rule.

So that the circuit becomes,

Thus,

$$V_{BC} \rightarrow V_T = I_B R_B + V_{BE} + I_E R_E$$

$$= I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$I_E = I_B + I_C$$
\[ V_T = I_B (R_B + R_E) + V_{BE} + I_C R_E \]

\[ V_{BE} = V_T - I_B (R_B + R_E) + I_C R_E \quad \rightarrow \quad 5 \]

To find \( I_B \):

From equation (5),

\[ I_B = \frac{V_T - V_{BE} - I_C R_E}{R_B + R_E} \quad \rightarrow \quad 6 \]

To find \( S \):

\[ I_C = \beta I_B + (1 + \beta) I_{CBO} \]

\[ I_B = \frac{I_C - (1 + \beta) I_{CBO}}{\beta} \quad \rightarrow \quad 7 \]

WK\( T \)

\[ \frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_B + R_E} \]

\[ S = \frac{(1 + \beta)}{(1 - \beta)} \frac{-R_E}{R_B + R_E} \]

\[ = \frac{(1 + \beta)}{(1 - \beta)} \frac{-R_E}{R_B + R_E} \]

\[ S = \frac{(1 + \beta)(R_B + R_E)}{R_B + R_E + \beta R_E} \]

\[ S = \frac{(1 + \beta)(R_B + R_E)}{R_B + (\beta + 1)R_E} \quad \rightarrow \quad 8 \]

To find \( S' \):

\[ \frac{\partial I_C}{\partial V_{BE}} \]

From equation (7),

\[ V_{BE} = V_T + I_B (R_B + R_E) - I_C R_E \]

Sub equation (7),

\[ V_{BE} = V_T + \frac{I_C - (1 + \beta) I_{CBO}}{\beta} (R_B + R_E) - I_C R_E \]
Let

\[ V'_s = \frac{(1 + \beta) I_{CEO}(R_B + R_E)}{\beta} \]

\[ V_{BE} = V_T + \frac{l_c(R_B + R_E(1 + \beta))}{\beta} + V' \]

\[ \frac{l_c(R_B + R_E(1 + \beta))}{\beta} = V_T - V_{BE} + V' \]

\[ I_c = \frac{\beta[V_T - V_{BE} + V']}{R_B + (\beta + 1)R_E} \quad \rightarrow \quad 9 \]

\[ s'S' = \frac{\partial I_c}{\partial V_{BE}} = -\frac{\beta}{R_B + (\beta + 1)R_E} \quad \rightarrow \quad 10 \]

To find \( S'' \):

\[ S'' = \frac{\partial I_c}{\partial \beta} \]

Differentiating equation (9), WRT \( \beta \)

\[ S'' = \frac{R_B + R_E(1 + \beta)[V_T - V_{BE} + V'] - \beta[V_T - V_{BE} + V']R_E}{[R_B + R_E(1 + \beta)]^2} \]

\[ S'' = \frac{(R_B + R_E)[V_T - V_{BE} + V']}{[R_B + R_E(1 + \beta)]^2} \]

Now multiply and divide by \( (1 + \beta) \)

\[ S'' = \frac{(R_B + R_E)[V_T - V_{BE} + V']}{[R_B + R_E(1 + \beta)]^2} \times \frac{(1 + \beta)}{(1 + \beta)} \]

\[ S'' = \frac{s[V_T - V_{BE} + V']}{(1 + \beta)R_B + R_E(1 + \beta)} \]

\[ S'' = \frac{l_cS}{\beta (1 + \beta)} \text{ by equation (9)} \quad \rightarrow \quad 11 \]
Relation between S and S’

\[ S = \frac{(1 + \beta)(R_B + R_E)}{R_B + (\beta + 1)R_E} \]

\[ S' = \frac{-\beta}{R_B + (\beta + 1)R_E} \]

Multiply and divide by \((1 + \beta)(R_B + R_E)\)

\[ S' = \frac{-\beta}{(1+\beta)(R_B+R_E)} \times \frac{(1 + \beta)(R_B + R_E)}{(1 + \beta)(R_B + R_E)} \]

\[ S' = \frac{-\beta S}{(1+\beta)(R_B+R_E)} \to 12 \]

Relation between S and S’

\[ S'' = \frac{I_C S}{\beta(1+\beta)} \text{ by equation (11)} \]

**BIAS COMPENSATION:**

Compensation techniques use temperature sensitive devices such as diode, transistors, thermistors, sensistors etc. to maintain operating point constant.

**THERMISTOR COMPENSATION:**

Thermistors have a negative temperature co-efficient ie. Its resistance decrease exponentially with increase in temperature as shown below.

Slope of this curve = \(\frac{\partial R_T}{\partial T}\)

Where \(\frac{\partial R_T}{\partial T}\) \(\to\) temperature coefficient for thermistor.

It is negative.

Therefore, thermistors are said to have negative temperature coefficient of resistance (NTC).
FIRST TYPE:

COMPENSATION TECHNIQUE:

Consider the circuit shown below.

Here in the circuit, \( R_T \) is \( R_b \) (Thermistor resistor), which has NTC.

When temperature increase

\[ R_T \text{ decreases} \quad \quad I_c \text{ increases} \]

\[ V_B \text{ decreases (drop across } R_T \text{)} \]

\[ V_{BE} \text{ decreases } (V_B = V_{BE} + V_E) \]

\[ I_s \text{ decreases} \]

\[ I_c \text{ decreases} \quad \text{since } I_c = \beta I_B \]

\[ I_c = \beta I_B \]

Thus the original increase in \( I_c \) is compensated and Q-Point is made stable.
SECOND TYPE:

Explanation:

When temperature increases

- $R_T$ decreases, $I_C$ increases
- $I_E$ increases
- $V_E$ increases
- $V_{BE}$ decreases ($V_E - V_B = V_{EB}$)
- $I_B$ decreases
- $I$ decreases

Thus the original increase in $I_C$ is compensated and Q-Point is maintained.

Sensistor compensation technique:

Sensistors have a positive temperature co-efficient ie. Its resistance increase with increase in temperature as shown.
Where \( \frac{\Delta R_T}{\Delta T} \) = temperature co-efficient

= is positive

Thus the variation in \( I_c \) is compensated.
DIODE COMPENSATION FOR $V_{BE}$:

Thus the variation in $V_{BE}$ is cancelled due to $V_{D}$ *(Reverse polarity)*

$$V_{BE} = V + I_B R_B + V_E + V_D$$

$$V = I_B R_B + V_E - V_D$$

Temperature increases

$V_{BE}$ increases

$V_D + V_{EB}$ as it is forward biased

$I_C$ increases

By 2.5 mV/°C
DIODE COMPENSATION FOR $I_{CO}$

\[ I = \frac{V_{CC} - V_{BE}}{R_1} \]

\[ I = \frac{V_{CC}}{R_1} [V_{BE} \approx 0.2 \text{ for } Ge] \]

\[ I_B = I + I_d \]

WKT,

\[ I_C = \beta I_B + (1 + \beta) I_{CBO} \]

\[ I_C = \beta (I - I_d) + (1 + \beta) I_{CBO} \]

\[ I_C = \beta I - \beta I_d + \beta I_{CBO} + I_{CBO} \]

FET BIASING:

The general relationship that can be applied to the DC analysis of all FET amplifiers are

\[ I_q \approx 0A \]

\[ I_D = I_S \]

For JFETS and depletion – type MOSFETS shockley’s equation is applied to relate the input and output quantities:

\[ I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2 \]

For enhancement – type MOSFET’S the following equation is applied:
\[ I_D = K((V_{GS} - V_T)^2) \]

Where
\( I_{DD} \) – Reverse saturation current
\( V_P \) – Pinch of voltage

**FIXED BIAS CONFIGURATION**

Consider the configuration shown below which includes the AC levels \( v_i \) and \( V_O \) and the coupling capacitors (\( C_1 \) and \( C_2 \)).

For DC analysis, capacitors acts like open circuit ie. At DC, \( f = 0 \), capacitance \( = \frac{1}{j\omega C} = \alpha \)

For AC analysis, capacitors acts like short circuits.

The resistors \( R_0 \) is to ensure that \( V_i \) appears at the input to the FET amplifier for AC analysis.

For dc analysis, \( I_G \cong 0A \)

\[ V_{RG} = I_G R_G = 0 \]

Replace \( R_C \) by short circuit in the circuit.

\[ V_{Ra} = I_R R_a = 0 V \]
To find $V_{GS}$

Apply KVL to gate circuit,

$$-V_{GG} = V_{GS}$$

$$V_{GS} = -V_{GG} \rightarrow 1$$

Since $V_{GG}$ is fixed DC supply the voltage $V_{GS}$ is fixed in magnitude, resulting in the notation "fixed bias configuration".

To find $I_D$:

$I_D$ is controlled by shockley's equation,

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$
SELF BIAS CONFIGURATION

This eliminates the need for two DC suppliers.

DC analysis:

For DC analysis, capacitors are replaced by ‘open circuits’ and the resistors $R_G$ replaced by short – circuit since $I_G = 0A$.

Therefore the circuit reduce to,

To find $V_{GS}$:

apply KVL to gate circuit,

$V_{GS} + V_{RS} = 0$

$V_{GS} = -V_{RS}$
\[ V_{GS} = -I_D R_S \quad \rightarrow 1 \]

\[ V_{CS} \rightarrow \text{Function of } I_D \text{ and not fixed as in fixed bias.} \]

To find \( I_D \):

by shockley's equation,

\[ I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 \]

\[ I_D = I_{DSS} \left( 1 - \frac{-I_D R_S}{V_P} \right)^2 \]

\[ I_D = I_{DSS} \left( 1 + \frac{I_D R_S}{V_P} \right)^2 \quad \rightarrow 2 \]

To find \( V_{DS} \):

Apply KVL to output circuit,

\[ V_{DD} = I_D R_D - V_{DS} + I_S R_S \]

\[ I_S = I_D \]

\[ V_{DD} = I_D R_D - V_{DS} + I_D R_S \]

\[ V_{DD} = I_D (R_D + R_S) + V_{DS} \]

\[ V_{DS} = V_{DD} - I_D (R_D + R_S) \quad \rightarrow 3 \]

**VOLTAGE – DIVIDER BIASING:**

Consider the circuit shown.
DC analysis:
  → Remove the AC source
  → O.C all the capacitors.

So that the circuit reduce to

From the circuit,

\[ V_G = \frac{V_{DD}R_2}{R_1+R_2} \rightarrow 1 \]

By voltage divider sub

To find \( V_{GS} \):

apply KVL to gate circuit,

\[ V_G = V_{GS} + V_{RS} \]
\[ V_G = V_{GS} + I_S R_S \]
\[ V_G = V_{GS} + I_D R_S \]
\[ I_S = I_D \]
\[ V_{GS} = V_G - I_D R_S \rightarrow 2 \]

To find \( V_{DS} \):

Apply KVL to drain circuit,

\[ V_{DD} = I_D R_D - V_{DS} + I_S R_S \]
\[ V_{DD} = I_D (R_D + R_S) + V_{DS} \]
\[ I_D = I_S \]
\[ V_{DS} = V_{DD} - I_D (R_D + R_S) \rightarrow 3 \]